Integrated HV Power MOSFET Quasi-Resonant PWM Controller for Fly-Back Converters

DESCRIPTION

ETA8051 is a high performance peak current mode PWM controller. It integrates a 1.3Ω/700V high reliability and high stability N-channel Power Mosfet. ETA8051 employs Quasi-Resonant and frequency fold-back technique to reduce EMI and improve average efficiency and meets the latest Level VI efficiency standard with enough margins.

ETA8051 is a multi-mode QR/CCM controller. In full load conditions, ETA8051 can work in both CCM mode and DCM mode to meet different types of applications. Quasi-Resonant (QR) function works all the time in DCM modes. Its burst mode operation enables low standby power with small output voltage ripple. And it achieves very low standby power, good dynamic response and accurate voltage regulation with an opto-coupler and the secondary side control circuit.

With build-in fast start process, ETA8051 can get output voltage very short rise time even with a big capacitive load. And a soft start circuit keeps output voltage no overshoot at power up.

ETA8051 integrates comprehensive protection. In case of over temperature, input/output over voltage, winding short, current sense resistor short, over load and over current and output short conditions, it would enter into auto restart if recovering from fault mode. Cycle-by-Cycle current limiting ensures safe operation even during fault mode and recovering.

ETA8051 is for applications up to 15 Watts.

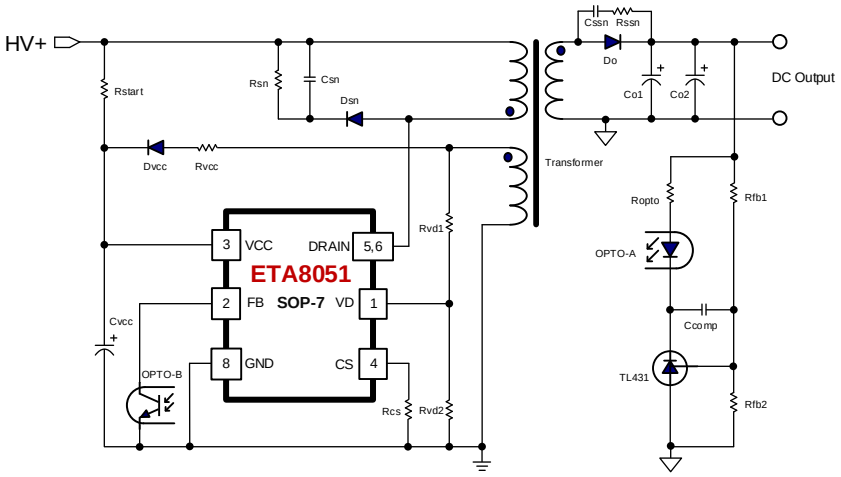
FEATURES

- Integrated 1.3Ω/700V high voltage N-channel Power Mosfet
- Quasi-Resonant and CCM Operation
- 7-37V VCC Widely Operation Voltage Range
- Built-in Adjustable Line Compensation
- Current Sense Resistor Short Protection
- Transformer Winding Short Protection
- Integrates Comprehensive Protection
- Built-in Soft-Start and Fast-Start Circuit
- Very Low Standby Power Consumption
- Complies with DOE VI and CEC V5 Average Efficiency Standards
- Standard SOP-7 Package

APPLICATIONS

- Smart Power Meters
- Conventional Adapter
- System Standby Powers
- Replacements for linear transformers and RCC SMPS

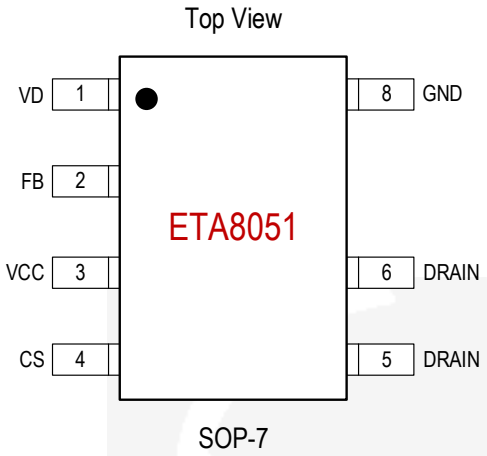
TYPICAL APPLICATION



ORDERING INFORMATION

PART No.	PACKAGE	TOP MARK	Pcs/Reel
ETA8051S7A	SOP-7	ETA8051 YWW2L	4000

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

(Note: Exceeding these limits may damage the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.)

DRAIN to CS .....–0.3V to +650V
FB,VD to GND .....–0.3V to +6V
VCC, CS to GND .....–0.3V to 40V
Maximum Power Dissipation (SOP-7) 1.5W
Operating Temperature Range .....–40°C to 105°C
Storage Temperature Range.....–55°C to 150°C
Thermal Resistance θ_{JC} θ_{JA}
SOP-7.....45.....75.....°C/W
Lead Temperature (Soldering 10Sec) .....260°C
ESD HBM (Human Body Mode) 2KV

ELECTRICAL CHARACTERISTICS

(V_{CC} =15V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply					
VCC Turn-On Voltage	VCC Rising From 0V	16.5	18	19.5	V
VCC Turn-Off Voltage	VCC Falling after Turn-on	6.5	7.0	7.5	V
VCC Over-Voltage Protection Voltage	VCC Rising From 0V	37	41	43	V
VCC Input Supply Current	Vcc=15V, Before VCC Turn-on		7	14	μA
	Vcc=25V, After VCC Turn-on, Loading		0.7	1	mA
	Vcc=15V, After VCC Turn-on, No load		0.3	0.4	mA
	Vcc=15V, Fault mode		0.2	0.3	mA
HV Section(DRAIN PIN)					
Power Mosfet Drain-Source Breakdown Voltage	V_{GS}=0V, I_{DS}=250μA,T_j=25°C	700			V
Power Mosfet Drain-Source on Resistor	V_{GS}=10V, I_{DS}=3A,T_j=25°C		1.3	1.5	Ω

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Power Mosfet Drain-Source Leakage Current	V_{DS}=650V, V_{GS}=0V,T_j=25°C			1	μA
Power Mosfet Source-Drain Diode Forward Voltage	V_{GS}=0V, I_{DS}=3A,T_j=25°C		1.3		V
Feedback					
FB Pull Up Resistor			16		kΩ
Vfb Max Value	OLP	4.5	4.85		V
OLP Blanking Time			160		mS
FB Threshold to Stop Switching	V_{FBOFF}	1.75	1.85	1.95	V
FB Threshold to Start Switching	V_{FBON}	1.8	1.9	2	V
Current Sense					
CS Voltage Limit Threshold		0.91	0.97	1.03	V
CS Leading Edge Blanking Time			300		nS
CS Short Voltage Threshold			0.1	0.125	V
CS Short Detection Waiting Time			2		μS
CS Open Voltage Threshold		1.5	1.75		V
CS to FB Gain			3		V/V
Oscillator					
Full Load Switching Frequency			75		kHz
Maximum Switching Frequency	F_{MAX}	80	85	90	kHz
Switching Frequency Foldback		26	29	32	kHz
Valley Detection					
ZCD Threshold Voltage			150		mV
Valley Detection Time Window	No valley detected force turn-on		3		μS
VD Over Voltage Threshold		3.0	3.15	3.3	V
VD Under Voltage Threshold	For output short circuit		0.6		V
VD Under Voltage Protection Waiting Time	For output short circuit		6		mS
Input Over Voltage Detection Threshold	$I_{VD,}$ Four cycle delay		2.5		mA
Input Under Voltage Detection Threshold	$I_{VD,}$ Four cycle delay		25		μA
Other Parameters					
Soft-Start Time			1.6		ms
Over Temperature Protection			135		°C
OTP Thermal Hysteresis			30		°C

PIN DESCRIPTION

PIN #	NAME	DESCRIPTION
1	VD	Valley Detection. Connect this pin to a resistor divider network from the auxiliary winding to ground to detect zero-crossing points for valley turn on operation. Line compensation and line UVLO and OVP all are integrated in VD pin.
2	FB	Feedback Pin. Connect OPTO to ground.
3	VCC	Power Supply. This pin provides bias power for the IC during startup and steady state operation.
4	CS	Current Sense Pin. Connect an external resistor (RCS) between this pin and ground to set peak current limit for the primary switch. The peak current limit is set by 0.97V / RCS.
5,6	DRAIN	HV power Mosfet Drain Pin. The DRAIN Pin is connected to the primary lead of the transformer.
8	GND	Ground.

FUNCTIONAL DESCRIPTIONS

ETA8051 meets the green-power requirement and is intended for the use in those modern switching power suppliers and adaptors which demand higher power efficiency and power-saving. It integrated the most advance features to reduce the external components counts and the size. Its major features are described as below.

VCC Under Voltage Lockout (UVLO) and Over Voltage Protection (OVP)

An UVLO protection is implemented in ETA8051 to detect the voltage on the VCC pin. It would assure the supply voltage enough to turn on the PWM controller and further to drive the internal power Mosfet. ETA8051 is implemented an OVP function on Vcc Pin to prevent spike voltage damage IC. An internal 12V clamp circuit is used to protect the gate of power MOSFET for high Vcc, as the max MOSFETs gate's Vgs nowadays are often limited to 30V. ETA8051 Gate clamp circuit also improves EMI performance and system efficiency.

The Vcc UVLO and OVP function is an auto-recovery type protection. If the UVLO/OVP occurs, ETA8051 stops switching and enters hiccup mode. If the UVLO/OVP condition is removed, the Vcc will restart and get back to normal level and the output will automatically return to the normal operation.

Startup

During startup, the VCC is lower than UVLO threshold and not high enough to turn on the MOSFET. The Vcc capacitor Cvcc is charged by AC Line through Rstart. The startup current of ETA8051 is designed to be very low so that Vcc could be charged to Vcc_on threshold level easily and the device starts up quickly. The Vcc is refreshed by the energy from the auxiliary winding of the transformer every cycle. Carefully selecting the value of Rstart and Cvcc will optimize the power consumption and startup time. For a typical AC/DC adaptor with universal input range design, two 1MΩ, 1/8 W startup resistors could be used together with a VCC capacitor (4.7uF) to yield a fast startup and low power dissipation. During startup period, the IC begins to operate with internal soft start circuit which uses minimum Ipk to minimize the switching stresses for the main switch, secondary output diode and transformers. After about 1.6mS, the IC operates at maximum driver output to achieve fast output voltage rise time. When Vout reaches about 80% Vout , the IC operates with a'soft-landing' mode(decrease Ippk) to avoid output voltage overshoot.

Constant Voltage (CV) Mode Operation

In constant voltage operation, the ETA8051 regulates its output voltage through secondary side control circuit. The output voltage information is sensed at FB pin through OPTO coupling. When the secondary output voltage is above regulation, the TL431 increases OPTO's I-N current to cause the error amplifier output voltage decreases to reduce the switch current. When the secondary output voltage is below regulation, the TL431 decreases OPTO's I-N current to cause the error amplifier output voltage increases, making the switch current increase to bring the secondary output back to regulation. The output regulation voltage is determined by the following equations:

$$V_{o\_CV} = V_{REF\_TL431} \times (1 + \frac{R_{F1}}{R_{F2}})$$

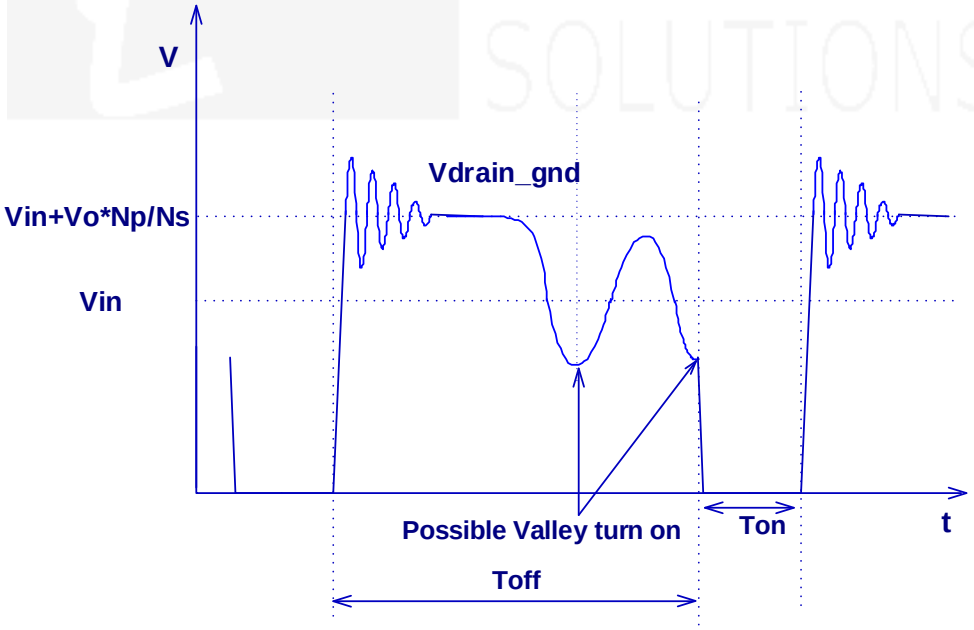
Where R_{F1} and R_{F2} are top and bottom feedback resistors of the TL431.

Over Current Protection (OCP) or Over Load Protection (OLP)

The ETA8051 shuts down when the power supply experiences an over current or over load. OCP/OLP is achieved by monitoring the FB voltage continuously. A fault signal is triggered when FB exceed typical value 4.5V and after a 160ms delay. If the fault signal is still present, the ETA8051 shuts down. When the fault disappears, the power supply resumes operation.

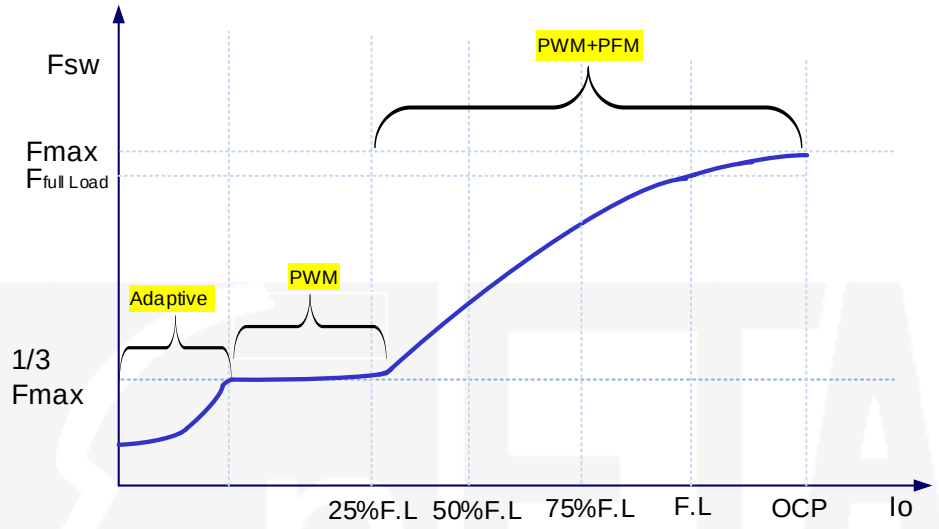
Valley Switching

ETA8051 employed valley switching from no load to heavy load to reduce switching loss and EMI when system is in discontinuous mode operation. After the switch is turned off, the ringing voltage from primary inductance and parasitic capacitance on MOSFET source pin is coupled by auxiliary winding and applied to the VD pin through feedback network Rvd1, Rvd2. Internally, the VD pin is connected to a zero-crossing detector to generate the switch turn on signal when the conditions are met.



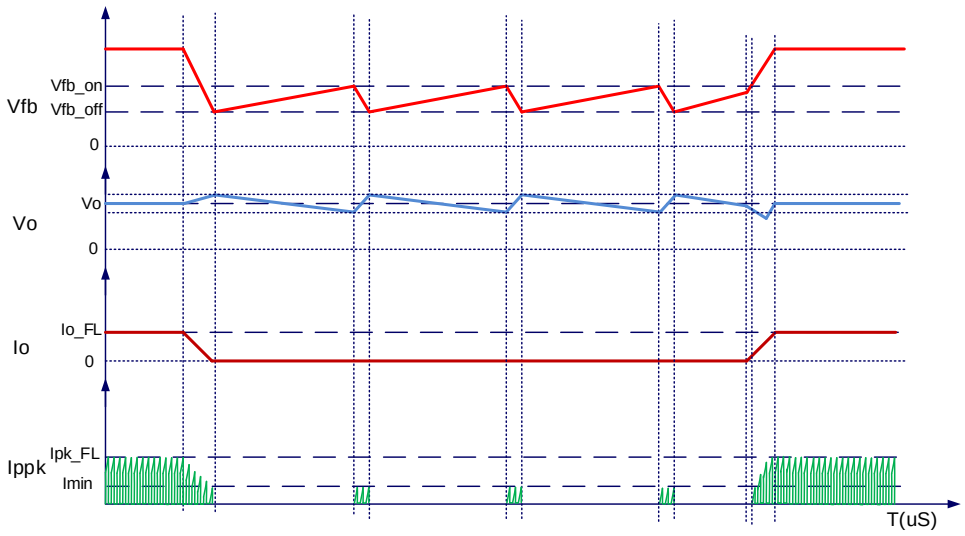
Frequency Foldback

When the load drops to 90% of full load level, ETA8051 starts to reduce the switching frequency which is proportional to the load current to improve the system average efficiency of the converter. The load adaptive switching frequency enables applications to meet all latest green energy standards. The actual minimum average switching frequency is programmable with output capacitance, feedback circuit and dummy load (while still meeting standby power).The actual frequency curve is as following:



Burst Mode In No Load

In standby mode, the feedback voltage oscillates between V_{FBON} and V_{FBOFF}. When Vfb decreases to V_{FBOFF}, ETA8051 stops switching. Then FB voltage will increases as Vout decrease gradually. When FB voltage reaches V_{FBON}, ETA8051 starts switching again. As Vout increase, Feedback voltage drops again and output voltage starts to bounds back and forth with very small output ripple because of very small delta voltage value of V_{FBON} -V_{FBOFF}. ETA8051 leaves burst mode when load is heavy enough to keep feedback voltage above V_{FBON}.



Primary Inductor Current Limit Compensation

The ETA8051 integrates a primary inductor peak current limit compensation circuit to achieve constant maximum power over wide line voltage. The compensation rate can be adjustable by the parallel resistor value of Rvd1 and Rvd2, the bigger the resistor, the smaller the compensation is.

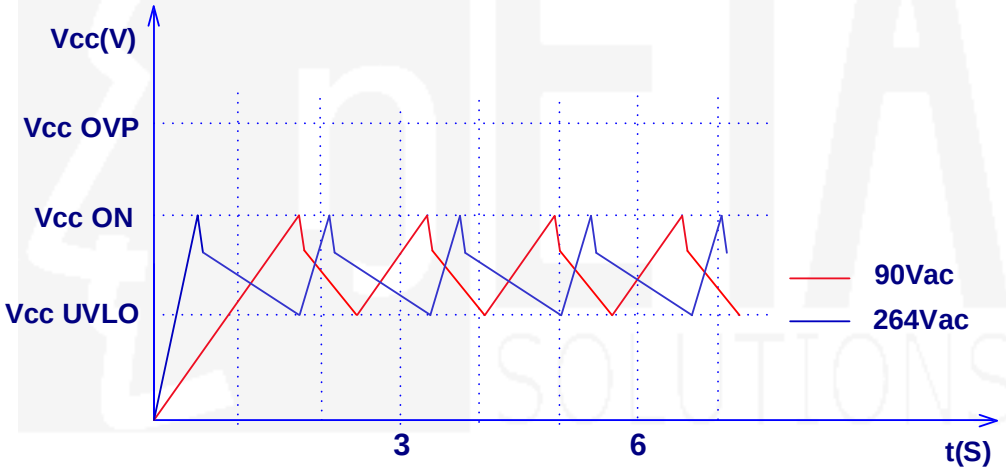
Slope Compensation

In the conventional application, the sub-harmonic oscillation is very severe in the current mode control when it operates in higher than 50% of the duty-cycle. ETA8051 has integrated fix slope compensation circuit inside.

Fault Protection

ETA8051 will enter into auto-restart mode to protect system when any fault is triggered. During startup, the detection of protection is inhibited for a period. After this period, miscellaneous protection is enabled. If there is no any protection triggered, the IC will startup normally, otherwise the IC will enter into protection mode. And normal operation proceeds once the failure mode is removed.

ETA8051 has implemented a startup delay time control to reduce the power loss during fault mode, the startup delay time increases over line voltage. The Vcc operation curve is as below:



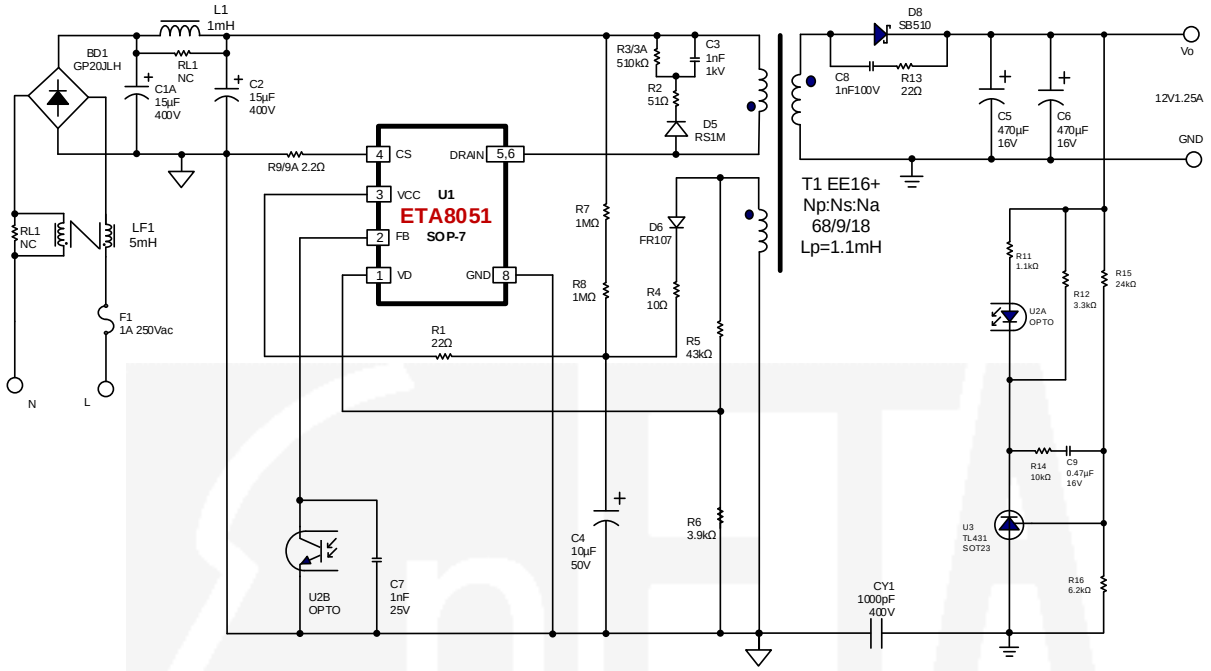
ETA8051 has integrated comprehensive fault protection which is listed in following table:

Protection Function	Failure Condition
Vcc OVP	Vcc>39V delay four switching cycles
Vcc UVLO	Vcc<7.0V delay four switching cycles
Vo OVP	Vvd>3.2V for four switching cycles
Line OVP	Ivd>2.5mA for four switching cycles
Line UVLO	Ivd<25uA for four switching cycles
Output Short (OSP)	Vvd<0.6V after 4 switching cycles after startup
Over Load/Over Current/Open Loop	Vfb=Max value (4.5V) for 160mS
Rcs Short	Vcs<0.1V after turn on 1uS
Rcs Open/ Primary Winding short/Output Schotkky short	Vcs>1.75V after turn on blanking time
Over Temperature (OTP)	Tdie_IC>135℃

APPLICATION INFORMATION

Schematic

Reference Application Circuit --- 15W (12V1.25A) adaptor:

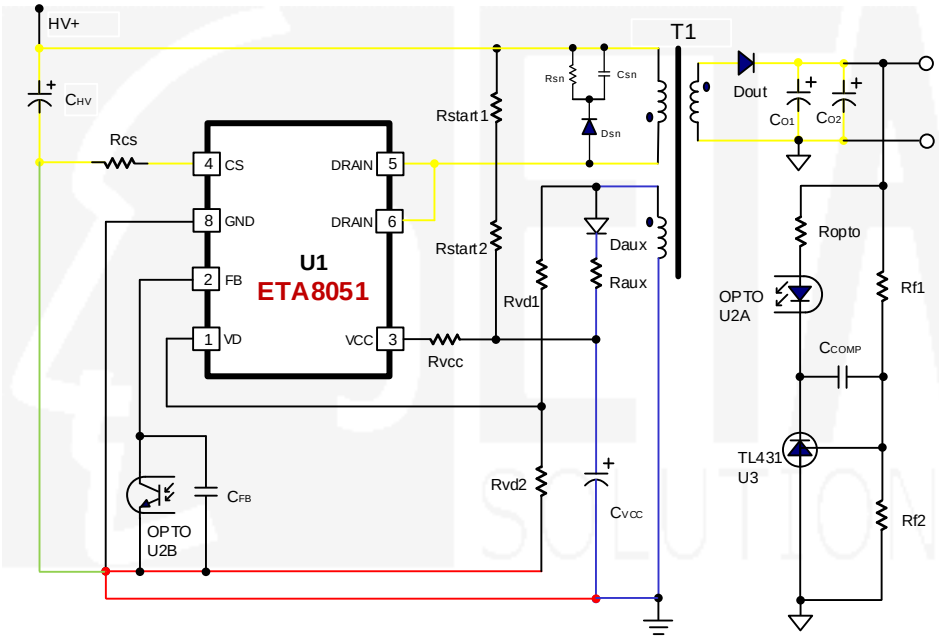


Bill of Materials

Item	Reference	Description	QTY	Manufacturer
1	U1	AC/DC PWM IC, ETA8051,SOP-7	1	ETA
2	U2	OPTO, EL817A,CTR:100~200%,DIP-4,	1	Ever-Light
3	U3	Ref IC, TL431A,Vref=2.5V,0.5%, SOT23	1	SK
4	F1	Fuse,1A/250V	1	Xcfuse
5	LF1	CM Inductor, 5mH, T9*6*3, 360mΩ，7448011305,	1	Wurth
6	L1	DM Inductor, 1mH, DR6*8, 100mΩ，7448012501	1	Wurth
7	CY1	Safety Y1,Capacitor,1000pF/400V,Dip,8853522110031	1	Wurth
8	BD1	KBP207,800V/2.0A,SOP4	1	PANJIT
9	C1,C1A	Capacitor, Electrolytic,15uF/400V, Φ10*12mm,865061463005	2	Wurth
10	C5,C6	Capacitor, Aluminum Electrolytic,470uF/16V, Φ8*12mm,870025374007	2	Wurth
11	T1	High Frequency Transformer, Lp=1.1mH, EE16+, Vertical	1	Fuzhou SY
12	D5	Fast Recovery Rectifier, RS1M,1000V/1.0A, RMA	1	MDD
13	D6	Fast Recovery Rectifier, FR107,1000V/1.0A, SOD-123F	1	MDD
14	D8	Schottky Diode Rectifier, MBR5100,100V/5A, Low Vf, RMA	1	Good-ark
15	C2	Capacitor, Ceramic, 10pF/25V, 0603,SMD, 885012006032	1	Wurth
16	C3	Capacitor, Ceramic, 1nF/500V, 1206,SMD,885012208075	1	Wurth
17	C4	Capacitor, Electrolytic,10uF/50V, 5x11mm,860240672002	1	Wurth
18	C7	Capacitor, Ceramic, 1nF/25V, 0603,SMD,885012206059	1	Wurth
19	C8	Capacitor, Ceramic, 1nF/100V, 0805,SMD, 885012207116	1	Wurth
20	C9	Capacitor, Ceramic,0.47uF/25V, 0603,SMD 885012206075	1	Wurth
21	R1	Chip Resistor, 22 ohm, 0603, 5%	1	UniOhm
22	R2	Chip Resistor, 51 ohm, 1206, 5%	1	UniOhm

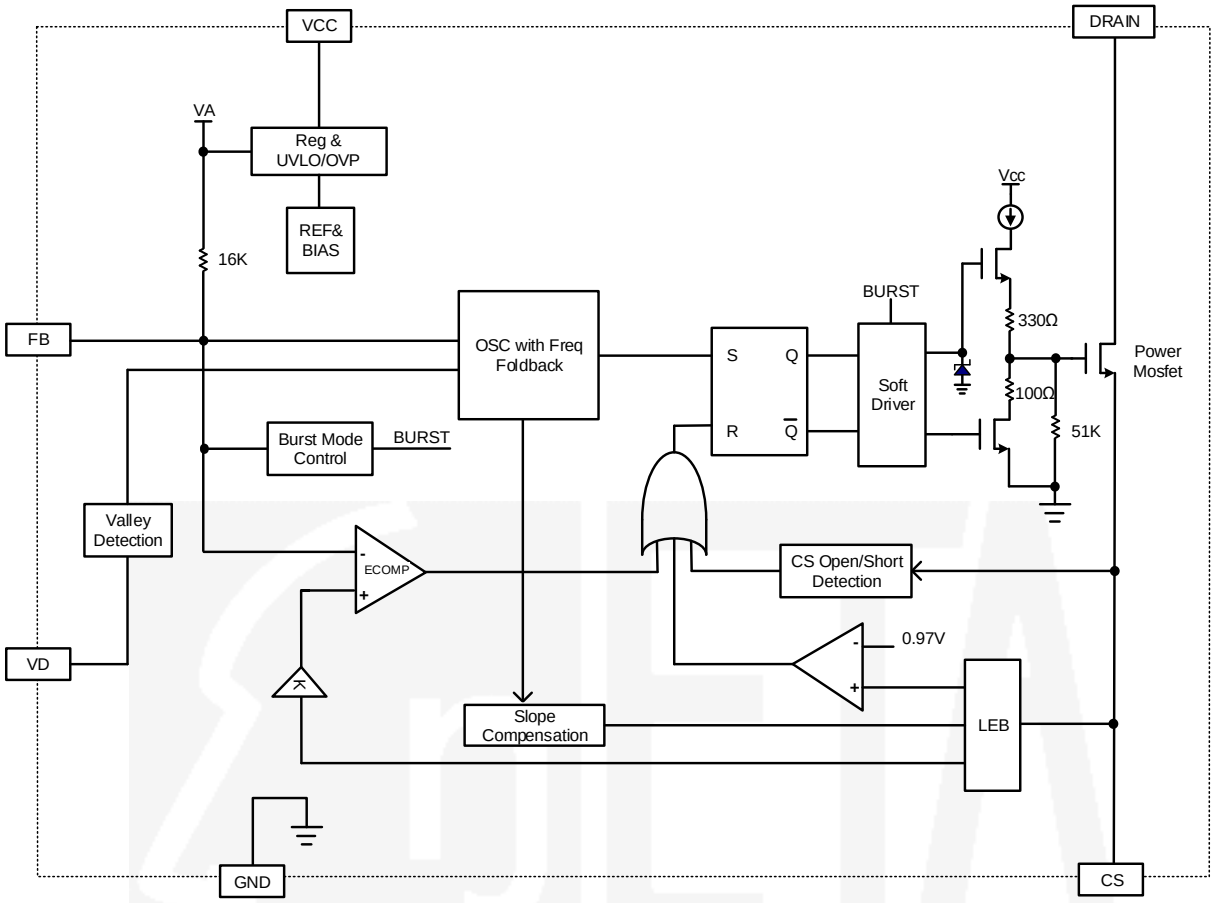
23	R3,R3A	Carbon Resistor, 510k ohm, 1206, 5%	1	UniOhm
24	R4	Chip Resistor, 10 ohm, 0805, 5%	1	UniOhm
25	R5	Chip Resistor, 43K ohm, 0603,1%	1	UniOhm
26	R6	Chip Resistor, 3.9K ohm, 0603, 1%	1	UniOhm
27	R7,8	Chip Resistor, 1M ohm, 0805, 5%	2	UniOhm
28	R9,9A	Chip Resistor, 2.2 ohm, 1206, 1%	2	UniOhm
29	R11	Chip Resistor, 1.1k ohm, 0603, 5%	1	UniOhm
29	R12	Chip Resistor, 3.3k ohm, 0603, 5%	1	UniOhm
30	R13	Chip Resistor, 22 ohm, 1206, 5%	1	UniOhm
31	R14	Chip Resistor, 10k ohm, 0603, 5%	1	UniOhm
32	R15	Chip Resistor, 24k ohm, 0603, 1%	1	UniOhm
33	R16	Chip Resistor, 6.2k ohm, 0603, 1%	1	UniOhm
34	PCB	FR-4, Single-sided Board, W*L*H=47mm*30mm*1.6mm	1	JDBPCB

PCB GUIDELINES



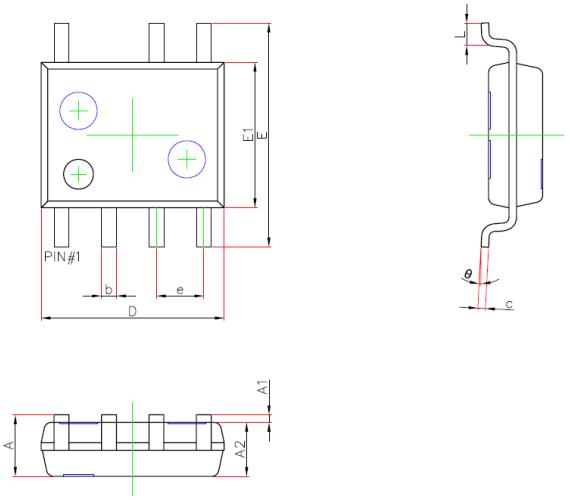
Good PCB layout is respectively to optimize IC and system performance. There are two main power path loops as above picture yellow wire. One is formed by C_{HV}, primary winding, ETA8051 power mosfet transistor and current sense resistor (Rcs). The other is secondary winding, rectifier Dout and output capacitors (Co1/Co2). The third small current path loop (Blue wire) is formed by auxiliary winding, rectifier Daux, filter resistor (Raux) and decoupling capacitors (Cvcc). Keep these loop areas as small as possible. Originated from the bulk capacitor (C_{HV}) ground, connecting high current ground returns and the ETA8051 signal GND PIN. Ground of detection resistor (Rvd1/Rvd2),OPTO(U2B), de-noising capacitor C_{FB} should directly connect to the ETA8051 ground(Red wire). Connecting the input capacitor (C_{HV}) ground lead, decoupling capacitors (Cvcc) returns, and the ETA8051 GND pin to a single point (ETA8051 star ground configuration).

BLOCK DIAGRAM



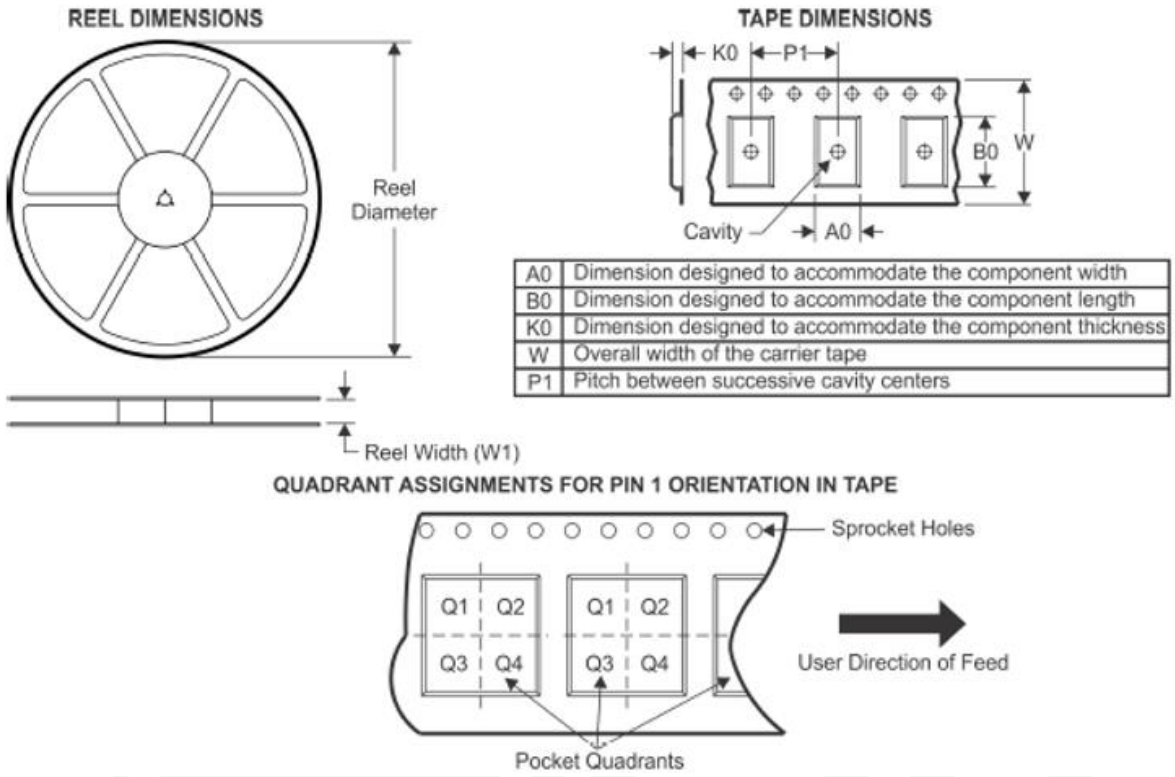
PACKAGE OUTLINE

Package: SOP-7



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.450	1.750	0.057	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.500	0.053	0.059
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ETA8051S7A	SOP-7	7	4000	330	12.7	6.6	5.4	2.05	8	12	Q1