3A 3MHz Synchronous Step-Down DC-DC in DFN3X3-10

FEATURES

- **High Efficiency: Up to 95%**
- **Capable of Delivering 3A**
- **Up to 3MHz Switching Frequency**
- **No External Schottky Diode Needed**
- **Low dropout 100% Duty operation**
- **Low Noise PWM control**
- **Programmable Frequency and Compensation Network**
- Internal Soft-Start
- Logic Control Shutdown (IQ<1uA)
- Thermal shutdown and UVLO
- Available in DFN-10

APPLICATIONS

- Portable Devices
- Cellular Base Stations
- Networking and Telecommunications
- 3G wireless Cards
- USB supplied Devices in Notebooks
- Distributed Power Systems

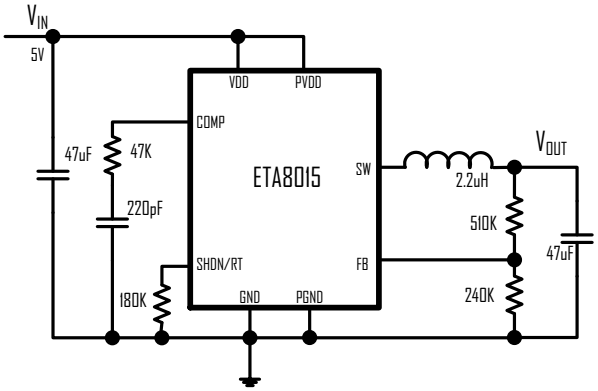
DESCRIPTION

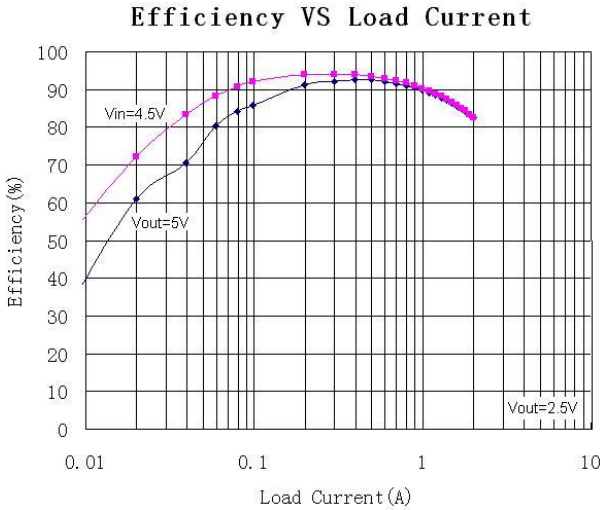
The ETA8015 is a high-efficiency, DC-to-DC step-down switching regulators, capable of delivering up to 3A of output current. The device operates from an input voltage range of 3.6V to 5.5V and provides an output voltage from 0.8V to VIN, making the ETA8015 ideal for low voltage power conversions. External programmable frequency and compensation network of the ETA8015 enable system designers to make trade off according to different requirements such as board space, output transient response and efficiency. Internal soft-start control circuitry reduces inrush current. Short-circuit and thermal-overload protection improves design reliability. ETA8015 is housed in a DFN-10 Package

ORDERING INFORMATION

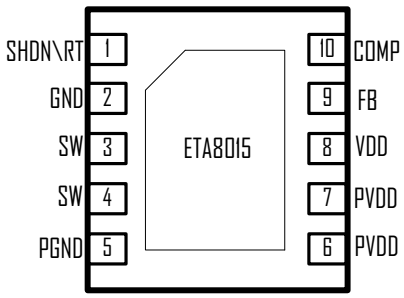
PART	PACKAGE PIN	TOP MARK
ETA8015D3K	DFN3x3-10	ETA8521-Product Number YWWPL — Date Code

TYPICAL APPLICATION





PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

(Note: Exceeding these limits may damage the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.)

VDD,PVDD,SW Voltage .....–0.3V to 6V
SHND\RT, FB, Comp Voltage .....–0.3V to 6V
SW to ground current .....Internally limited
Maximum Power Dissipation.....0.98W
Operating Temperature Range .....–40°C to 85°C
Storage Temperature Range .....–55°C to 150°C

ELECTRICAL CHACRACTERISTICS

(V_{IN} = 5V, unless otherwise specified. Typical values are at TA = 25oC.)

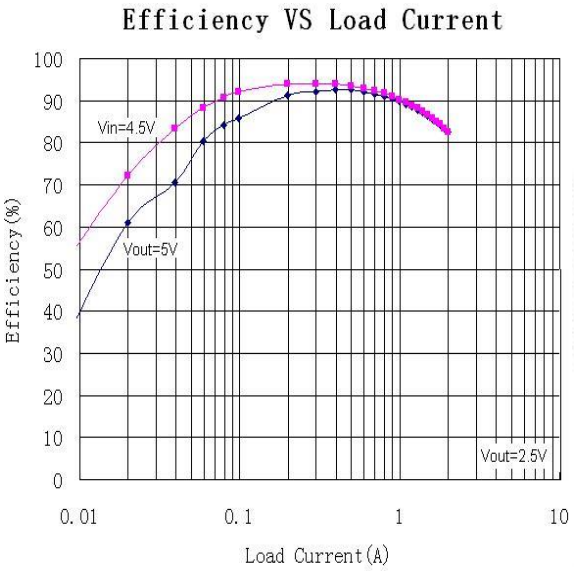
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range		3.6		5.5	V
Input UVLO	Rising, Hysteresis=100mV		2.5		V
Input Supply Current	V_{FB} =0.78V		420		μA
Input Shutdown Current				1	μA
FB Feedback Voltage	V_{OUT} =3.5 to 5V		0.8		V
FB Input Current			10		nA
Output Voltage Range		0.8		5	V
Load Regulation			0.1		%
Line Regulation	V_{IN} =2.7 to 5.5V		0.04		%/V
Error Amp Transconductance			300		μA/V
Current Sense Transresistance			0.2		Ω
Switching Frequency	Rosc=180K		1.8		Mhz
NMOS Switch On Resistance	I_{SW} =500mA		120		mΩ
PMOS Switch On Resistance	I_{SW} =500mA		90		mΩ
PMOS Switch Current Limit			4		A
NMOS Switch Current Limit			1		A
SW Leakage Current	V_{OUT}=5.5V,V_{SW}=0 or 5.5V,SHDN\RT= V_{IN}			10	μA
SHDN\RT Input Current				1	μA
SHDN\RT Input Low Voltage			V_{IN} – 0.4		V
SHDN\RT Input High Voltage			V_{IN} – 0.7		V
Thermal Shutdown Threshold	Rising, Hysteresis=20°C		160		°C

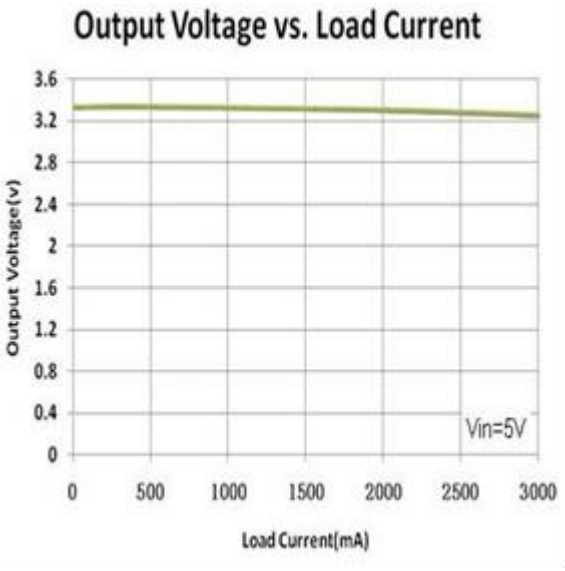
PIN #	NAME	DESCRIPTION
1	SHDN\RT	Oscillator Resistor Input. Connecting a resistor to ground from this pin sets the switching frequency. Forcing this pin to VDD causes the device to be shut down.
2	GND	Ground
3,4	SW	Inductor Connection. Connect an inductor Between SW and the regulator output.

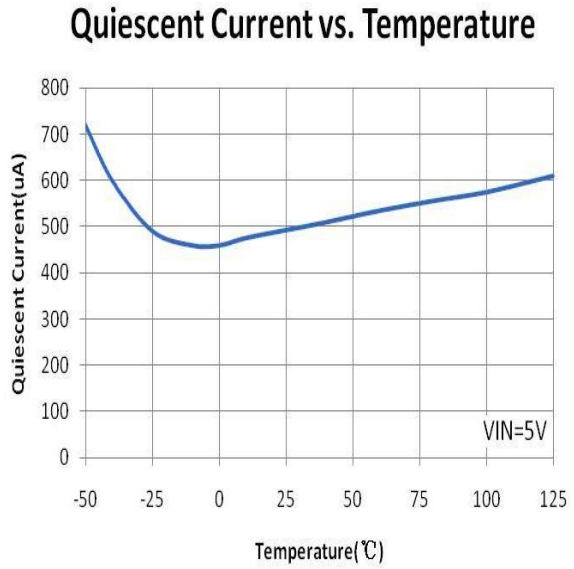
PIN #	NAME	DESCRIPTION
5	PGND	Power Ground. Connect to GND
6,7	PVDD	Power-Supply Voltage. Input voltage range from 3.6V to 5.5V. Bypass with a 22μF ceramic capacitor to PGND
8	VDD	Analog Supply Voltage. Short to PVDD. Bypass with a 22μF ceramic capacitor to GND
9	FB	Feedback Input. Connect an external resistor divider from the output to FB and GND to set the output to a voltage between 0.8V and VIN
10	COMP	Regulator Compensation. Connect series RC network to GND.

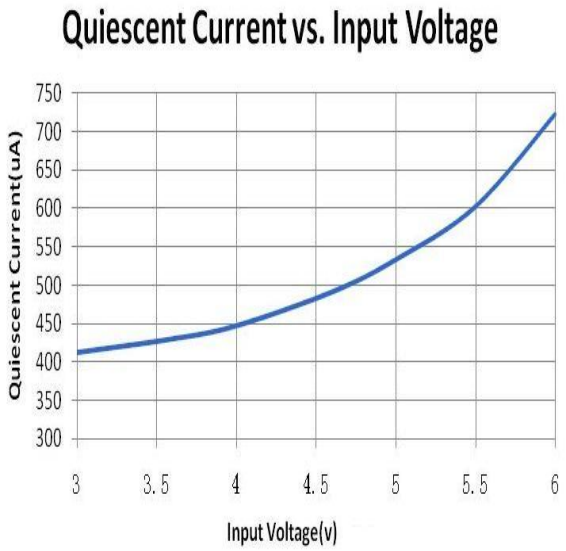
TYPICAL CHARACTERISTICS

(Typical values are at TA = 25oC unless otherwise specified..





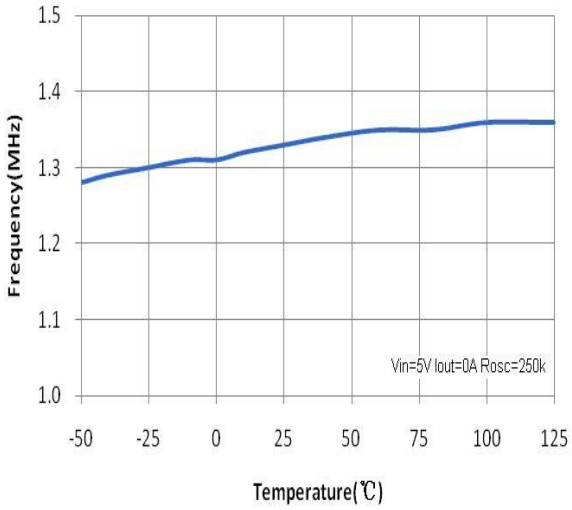




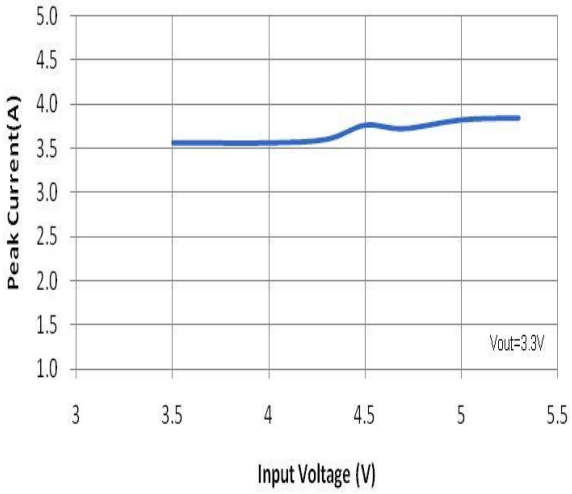
TYPICAL CHARACTERISTICS

(Typical values are at TA = 25oC unless otherwise specified..

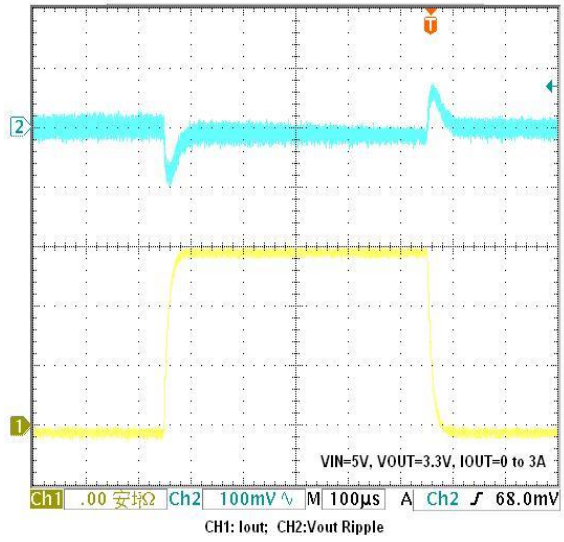
Frequency vs. Temperature



Peak Current vs. Input Voltage

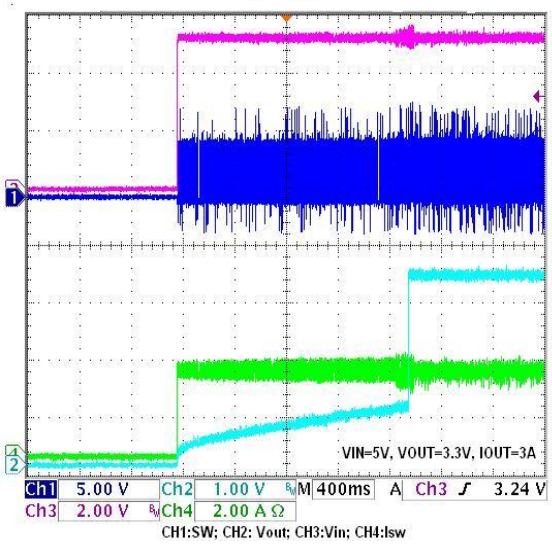


Load Transient Response



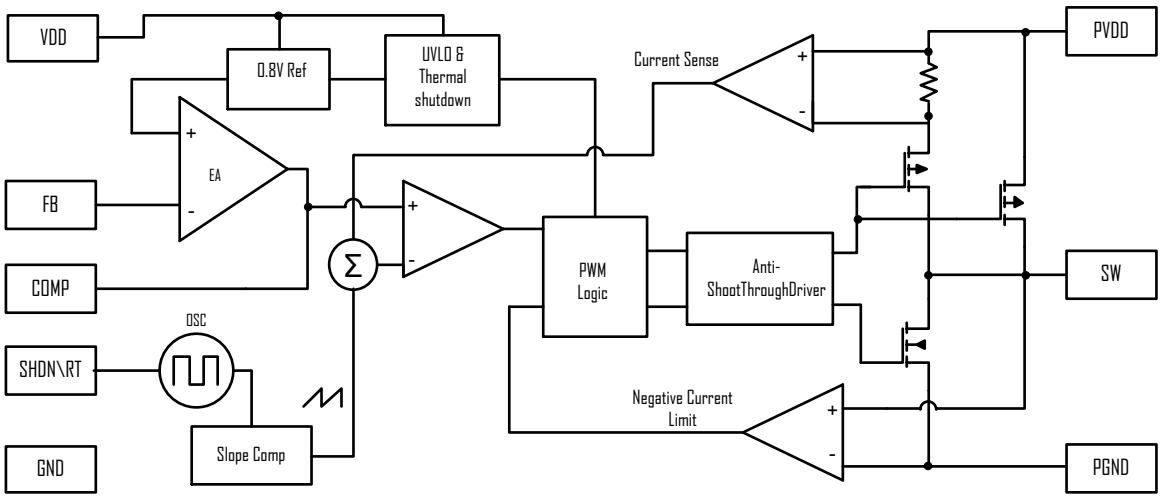
CH1: Iout; CH2:Vout Ripple

Soft Start



CH1:SW; CH2: Vout; CH3:Vin; CH4:Isw

BLOCK DIAGRAM



DETAIL DESCRIPTION

The ETA8015 high-efficiency switching regulator is a small, simple, DC-to-DC step-down converter capable of delivering up to 3A of output current. The device operates in pulse-width modulation (PWM) at a programmable frequency up to 3MHz from a 3.6V to 5.5V input voltage and provides an output voltage from 0.8V to VIN, making the ETA8015 ideal for on-board post-regulation applications. External programmable frequency and compensation network of the ETA8015 enable system designers to make trade off according to different requirements such as board space, output transient response and efficiency. An internal synchronous rectifier improves efficiency and eliminates the typical Schottky free-wheeling diode. Using the on resistance of the internal high-side MOSFET to sense switching currents eliminates current-sense resistors, further improving efficiency and cost.

Loop Operation

ETA8015 uses a PWM current-mode control scheme. An open-loop comparator compares the integrated voltage-feedback signal against the sum of the amplified current-sense signal and the slope compensation ramp. At each rising edge of the internal clock, the internal high-side MOSFET turns on until the PWM comparator terminates the on cycle. During this on-time, current ramps up through the inductor, sourcing current to the output and storing energy in the inductor. The current mode feedback system regulates the peak inductor current as a function of the output voltage error signal. During the off cycle, the internal high-side P-channel MOSFET turns off, and the internal low-side N-channel MOSFET turns on. The inductor releases the stored energy as its current ramps down while still providing current to the output.

Current Sense

An internal current-sense amplifier senses the current through the high-side MOSFET during on time and produces a proportional current signal, which is used to sum with the slope compensation signal. The summed signal then is compared with the error amplifier output (COMP) by the PWM comparator to terminate the on cycle.

Current Limit

There is a cycle-by-cycle current limit on the high-side MOSFET of 4A(typ). When the current flowing out of SW exceeds this limit, the high-side MOSFET turns off and the synchronous rectifier turns on. A negative current limit of 1A also protects the synchronous rectifier preventing large current flowing into SW. If the negative current limit is exceeded, the synchronous rectifier turns off, forcing the inductor current to flow through the high-side MOSFET body diode, back to the input, until the beginning of the next cycle

or until the inductor current drops to zero. ETA8015 utilizes a frequency fold-back mode to prevent overheating during short-circuit output conditions. The device enters frequency fold-back mode when the FB voltage drops below 300mV, limiting the current to 4A (typ) and reducing power dissipation. Normal operation resumes upon removal of the short-circuit condition.

Soft-start

ETA8015 has a digital soft-start circuitry to reduce supply inrush current during startup conditions. When the device exits under-voltage lockout (UVLO), shutdown mode, or restarts following a thermal-overload event, the digital soft-start circuitry slowly ramps up the voltages at REF and FB.

UVLO and Thermal Shutdown

If VDD drops below 2.5V, the UVLO circuit inhibits switching. Once VCC rises above 3.6V, the UVLO clears, and the soft-start sequence activates. Thermal-overload protection limits total power dissipation in the device. When the junction temperature exceeds TJ= +160°C, a thermal sensor forces the device into shutdown, allowing the die to cool. The thermal sensor turns the device on again after the junction temperature cools by 15°C, resulting in a pulsed output during continuous overload conditions. Following a thermal-shutdown condition, the soft-start sequence begins.

Design Procedure

Setting Switching Frequency

Choose a switching frequency to optimize external component size or circuit efficiency for the particular application. Typically, switching frequencies between 1MHz and 1.5MHz offer a good balance between component size and circuit efficiency—higher frequencies generally allow smaller components, and lower frequencies give better conversion efficiency. The switching frequency is set with an external timing resistor.and through the resistor connecting between SHDN\RT and GND. For typical frequency, Table 1 can be referred.

Table 1: Typical $R_{SHDN/RT}$ Value

$R_{SHDN/R}$ (kΩ)	180	220	330	660
Fre(MHz)	1.80	1.45	1.00	0.52

Setting Output Voltages

Output voltages are set by external resistors. The FB_ threshold is 0.8V.

$R_{TOP} = R_{BOTTOM}[(V_{OUT} / 0.8) - 1]$

General Filter Capacitor Selection

The input capacitor in a DC-to-DC converter reduces current peaks drawn from the battery or other input power source and reduces switching noise in the controller. The impedance of the input capacitor at the switching frequency should be less than that of the input source so high-frequency switching currents do not pass through the input source. The output capacitor keeps output ripple small and ensures control-loop stability. The output capacitor must also have low impedance at the switching frequency. Ceramic, polymer, and tantalum capacitors are suitable, with ceramic exhibiting the lowest ESR and high-frequency impedance. Output ripple with a ceramic output capacitor is approximately as follows:

$VRIPPLE = IL(PEAK)[1 / (2\pi \times f_{OSC} \times C_{OUT})]$

If the capacitor has significant ESR, the output ripple component due to capacitor ESR is as follows:

$V_{RIPPLE(ESR)} = IL(PEAK) \times ESR$

Inductor Selection

The external components required for the step-down are an inductor, input and output filter capacitors, and compensation RC network. ETA8015 provides best efficiency with continuous inductor current. A reasonable inductor value (LIDEAL) can be derived from the following:

$LIDEAL = [2(VIN) \times D(1 - D)] / IOUT \times fOSC$

This sets the peak-to-peak inductor current at 1/2 the DC inductor current. D is the duty cycle:

$D = VOUT / VIN$

Given LIDEAL, the peak-to-peak inductor current is 0.5 IOUT. The absolute-peak inductor current is 1.25 IOUT. Inductance

values smaller than LIDEAL can be used to reduce inductor size; however, if much smaller values are used, inductor current rises, and a larger output capacitance may be required to suppress output ripple. Larger values than LIDEAL can be used to obtain higher output current, but typically with larger inductor size.

Compensation

The relevant characteristics for step-down compensation are as follows:

- Transconductance (from FB to COMP), gmEA (300μS)
- Step-down slope-compensation pole, PSLOPE = VIN /(πL)
- Current-sense amplifier transresistance, RCS (0.2V/A)
- Feedback-regulation voltage, VFB (0.8V)
- Step-down output voltage, VSD, in V
- Output-load equivalent resistance, RLOAD=VOUT / ILOAD

The key steps for step-down compensation are as follows:

1) Set the compensation RC to zero to cancel the RLOAD COUT pole.

2) Set the loop crossover below the lower of 1/5 the slope compensation pole or 1/5 the switching frequency.

If we assume VIN = 5V, VOUT = 2.5V, and IOUT = 1000mA, then RLOAD = 2.5Ω.

If we select fOSC = 1000kHz and L = 2.2μH.

PSLOPE = VIN / (πL) = 723kHz, so choose fC = 140kHz and calculate CC:

CC = (VFB / VOUT)(RLOAD / RCS)(gm /(2π x fC))

= (0.8 / 2.5)(2.5 / 0.2) x [300μS / (6.28 x 140kHz)]

= 1.36nF

Choose 1.5nF.

Now select RC so transient-droop requirements are met. As an example, if 4% transient droop is allowed, the input to the error amplifier moves 0.04 x 0.8V, or 32mV. The error-amp output drives 32mV x 300μS, or 9.6μA across RC to provide transient gain. Since the current sense transresistance is 0.2V/A, the value of RC that allows the required load-step swing is as follows:

RC = 0.6 IIND(PK)*RCS / 9.6μA

In a step-down DC-to-DC converter, if LIDEAL is used, output current relates to inductor current by the following:

IIND(PK) = 1.25 IOUT

So for a 3A output load step with VIN = 5V and VOUT = 2.5V:

RC = (1.25 x 0.6 x 3 x0.2) / 9.6μA = 46.87kΩ

Choose 47kΩ.

Note that the inductor does somewhat limit the response in this case since it ramps at (VIN - VOUT) / 2.2μH, or (5 – 2.5) / 2.2μH = 1.136A/μs.

The output filter capacitor is then chosen so the COUT RLOAD pole cancels the RC CC zero:

COUT x RLOAD = RC x CC

For the example:

COUT = 47kΩ x 1.5nF / 2.5Ω = 28.2μF

Since ceramic capacitors are common in either 22μF or 47μF values, 22μF is within a factor of two of the ideal value and still provides adequate phase margin for stability. If the output filter capacitor has significant ESR, a zero occurs at the following:

ZESR = 1 / (2π x COUT x RESR)

If ZESR > fC, it can be ignored, as is typically the case with ceramic output capacitors. If ZESR < fC, it should be cancelled with a pole set by capacitor CP connected from CC to GND:

CP = COUT x RESR / RC

If CP is calculated to be <10pF, it can be omitted.

APPLICAITION INFORMATION

Layout is critical to achieve clean and stable operation. The switching power stage requires particular attention. Follow these guidelines for good PC board layout:

1) Place decoupling capacitors as close to the IC as possible. Keep power ground plane (connected to PGND) and signal ground plane (connected to GND) separate.

2) Connect input and output capacitors to the power ground plane; connect all other capacitors to the signal ground plane.

3) Keep the high-current paths as short and wide as possible. Keep the path of switching current (CI to IN and CI to PGND) short. Avoid vias in the switching paths.

4) If possible, connect IN, SW, and PGND separately to a large copper area to help cool the IC to further improve efficiency and long-term reliability.

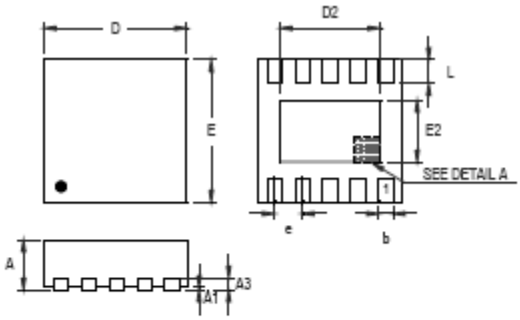
5) Ensure all feedback connections are short and direct. Place the feedback resistors as close to the IC as possible.
6) Route high-speed switching nodes away from sensitive analog areas (FB, COMP).

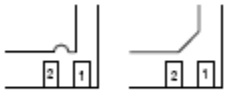
Thermal Considerations

ETA8015 uses a 10-pin DFN package with a RTHJC rating of 60°C/W. Thermal performance can be further improved with one of the following options:
1) Increase the copper areas connected to GND, SW, and IN.
2) Provide thermal vias next to GND and IN, to the ground plane and power plane on the back side of PC board, with openings in the solder mask next to the vias to provide better thermal conduction.
3) Provide forced-air cooling to further reduce case temperature.

PACKAGE OUTLINE

DFN10 PACKAGE OUTLINE AND DIMENSIONS





DETAIL A
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	2.300	2.650	0.091	0.104
E	2.950	3.050	0.116	0.120
E2	1.500	1.750	0.059	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018