18V, 3A, High Efficiency Synchronous Step-Down Converter

DESCRIPTION

ETA8103 is a wide input range, high-efficiency and high frequency DC-to-DC step-down switching regulator, capable of delivering up to 3A of output current. It adopts an adaptive COT control scheme that enables very fast transient response and provides a very smooth transition when the output varies from light load to heavy load.

The adaptive COT control also maintains a constant switching frequency across line and load. An OVP function protects the IC itself and its downstream system against input voltage surges. With this OVP function, the IC can stand off input voltage as high as 19V, making it an ideal solution for industrial applications such as LCD TV, Set Top Box, Portable TV, etc.

ETA8103 is available in SOT23-6 package.

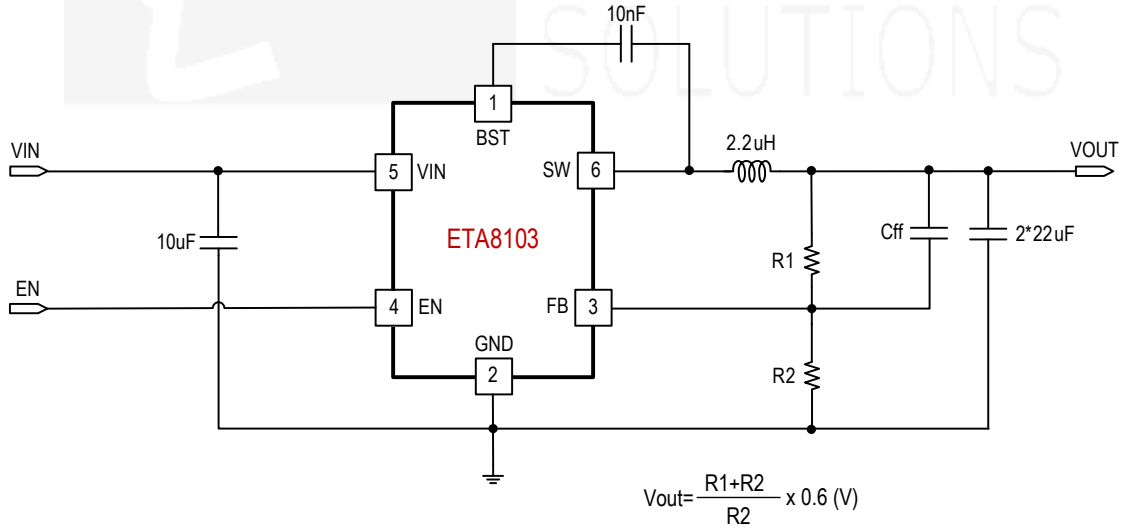
FEATURES

- Wide Input Range: 4V-18V
- Adaptive COT Control
- Ultra-Fast Load Transient Response
- Forced PWM Mode
- 1MHz Switching Frequency
- Low Rdson Internal Power FETs
- Capable of Delivering 3A
- No External Compensation Needed
- Thermal Shutdown and UVLO
- Available in SOT23-6 Package
- RoHS Compliant

APPLICATIONS

- Set Top Box
- LCD TV
- xDSL Modem

TYPICAL APPLICATION

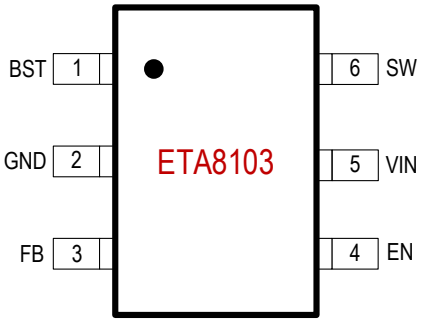


* R2 has to be between 1KOhm to 20KOhm

ORDERING INFORMATION

PART No.	PACKAGE	TOP MARK	Pcs/Reel
ETA8103S2G	SOT23-6	BRYW	3000

PIN CONFIGURATION



SOT23-6

ABSOLUTE MAXIMUM RATINGS

(Note: Exceeding these limits may damage the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.)

VIN,EN Voltage .....–0.3V to 19V
SW Voltage.....–0.3V (1) to 19V (2)
BST Voltage .....–0.3V to SW+6V
FB Voltage .....–0.3V to 6V
Junction Temperature ..... 150°C
Storage Temperature Range .....–55°C to 150°C

Thermal Resistance	θ_{JA}	θ_{JC}	
JESD51-3(3)	180	90	°C/W
EVB(4)	80	30	°C/W

Power Dissipation(5).....1.5W
Lead Temperature (Soldering 10sec) .....260°C
ESD HBM (Human Body Mode) 2KV
ESD CDM (Charged Device Mode) 1KV

Note:

(1) -5V for <10nS.
(2) 23V for <10nS.
(3) These values are calculated in accordance with JESD51-3 and simulated on a JEDEC board, they are only valid for comparison between different packages, cannot be used for thermal design.
(4) Measured on 1OZ two-layer ETA evaluation board ,TA=25°C； the top of SOT23-6 package is the position where θJC measured.
(5) Power Dissipation is calculated by PD=(Tjmax-Ta)/ θJA.

Recommended Operating Conditions

(Note: The device is not guaranteed to function outside its operating conditions.)

Ambient Temperature Range .....–40°C to 85°C
Junction Temperature Range .....–40°C to 125°C

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V, V_{OUT} = 3.3V, unless otherwise specified. Typical values are at TA = 25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage Range		4		18	V
Input UVLO	Rising, Hysteresis=320mV		3.7		V
Input OVP	Rising, Hysteresis=0.9V		19		V
Input Supply Current	V_{FB}=0.65V, no switching		230		μA
Input Shutdown Current			8	14	μA
FB Voltage		0.588	0.6	0.612	V
FB Input Current			0	1	μA
Switching Frequency			1000		kHz
Short Circuit Hiccup Time	On Time		1.5		mS
	Off Time		4.5		mS

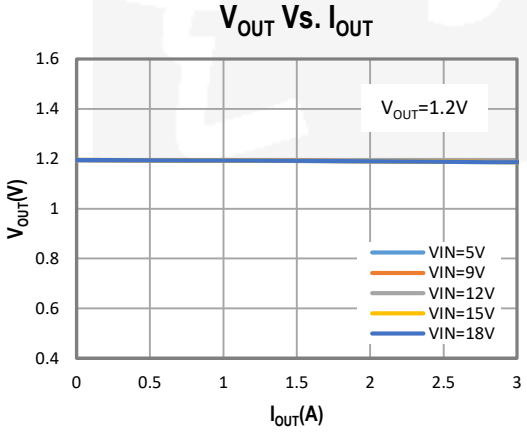
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
FB Hiccup Threshold			0.2		V
High Side Switch On Resistance			95		mΩ
Low Side Switch On Resistance			50		mΩ
High Side Current Limit			5		A
SW Leakage Current	V_{IN}=V_{SW}=12V, EN=GND			10	μA
EN Rising Threshold	Rising	1	1.2	1.4	V
EN Falling Threshold	Falling	0.9	1.1	1.3	V
EN Input Current	V_{EN}=2V		2	6	uA
Thermal Shutdown	Rising, Hysteresis =20°C		150		°C

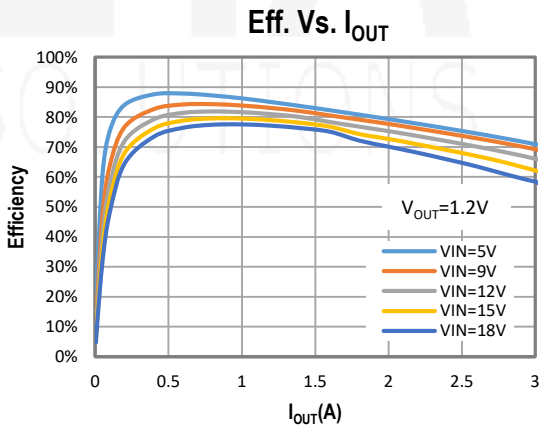
PIN DESCRIPTION

PIN #	NAME	DESCRIPTION
1	BST	Bootstrap pin. Connect a 10nF capacitor from this pin to SW
2	GND	Ground
3	FB	Feedback Input. Connect an external resistor divider from the output to FB and GND to set V_{OUT}
4	EN	Enable pin for the IC. Drive this pin high to enable the part, low or floating to disable.
5	VIN	Supply Voltage. Bypass with a 10μF ceramic capacitor to GND
6	SW	Inductor Connection. Connect an inductor between SW and the regulator output.

TYPICAL CHARACTERISTICS

(Typical values are at TA = 25°C unless otherwise specified.)

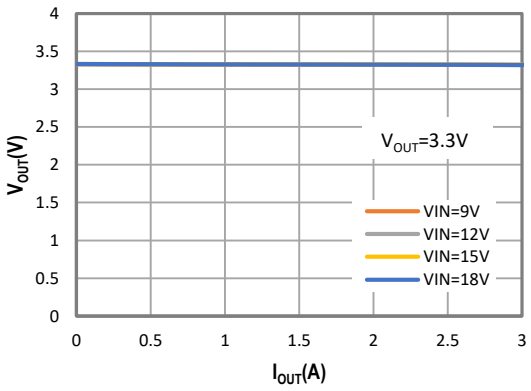




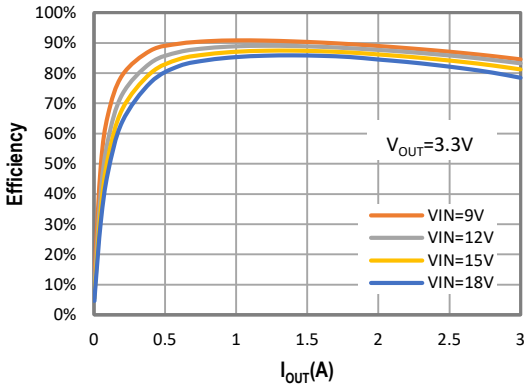
TYPICAL CHARACTERISTICS Cont'd

(Typical values are at TA = 25°C unless otherwise specified.)

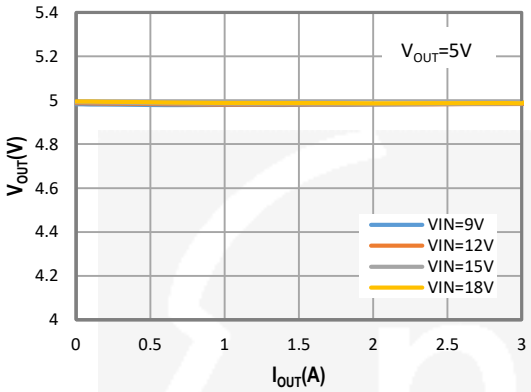
V_{OUT} Vs. I_{OUT}



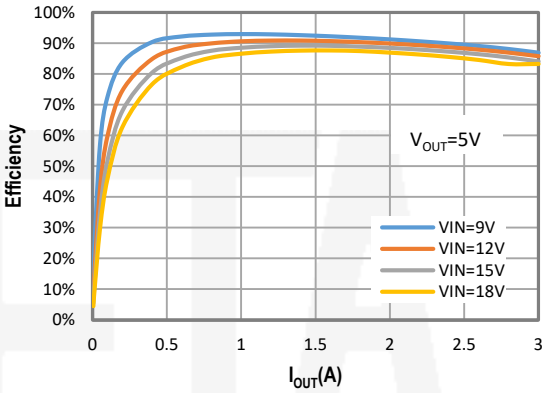
Eff. Vs. I_{OUT}



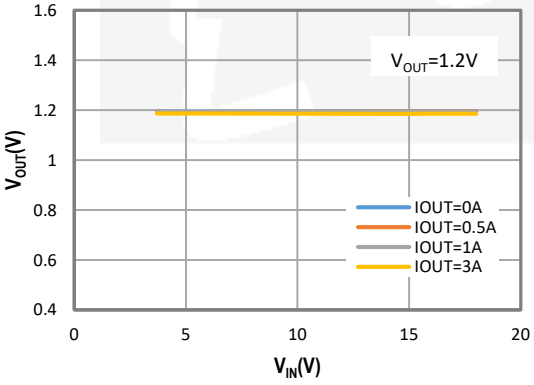
V_{OUT} Vs. I_{OUT}



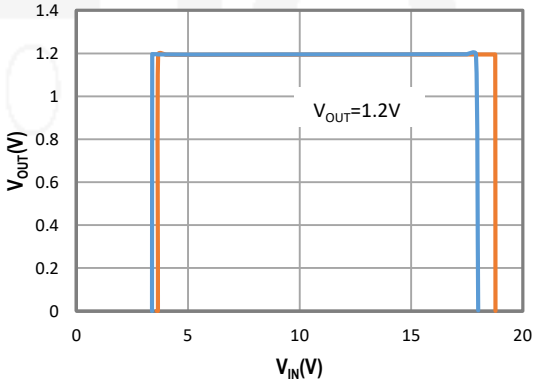
Eff. Vs. I_{OUT}



V_{OUT} Vs. V_{IN}



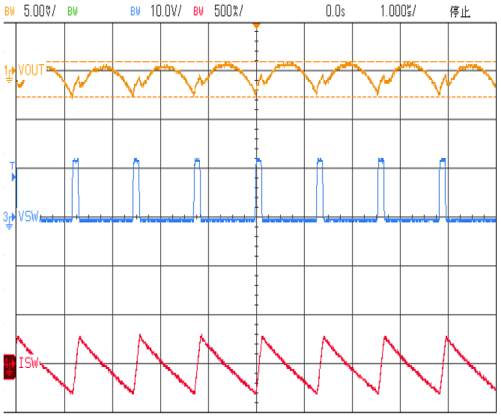
UVLO&OVP



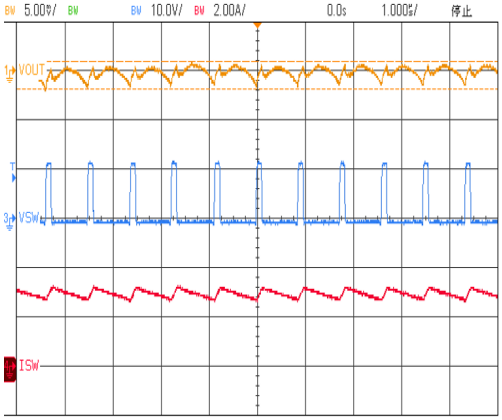
TYPICAL CHARACTERISTICS Cont'd

(Typical values are at TA = 25°C unless otherwise specified.)

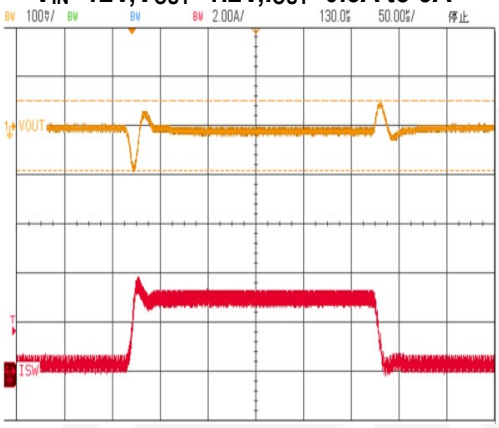
Output Voltage Ripple
V_{IN}=12V,V_{OUT}=1.2V,I_{OUT}=0A



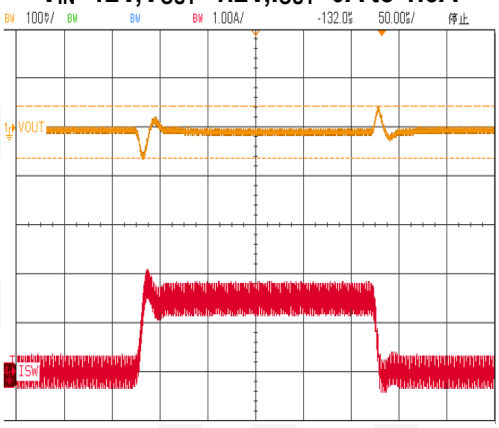
Output Voltage Ripple
V_{IN}=12V,V_{OUT}=1.2V,I_{OUT}=3A



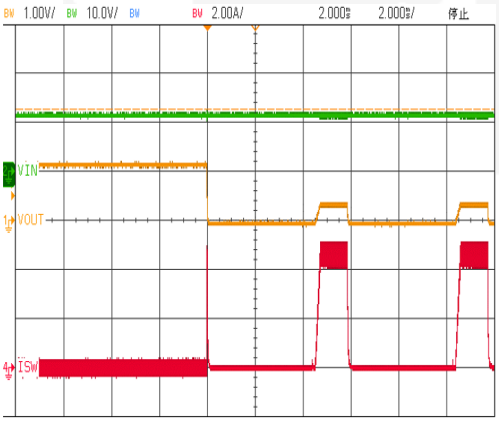
Load Transient
V_{IN}=12V,V_{OUT}=1.2V,I_{OUT}=0.3A to 3A



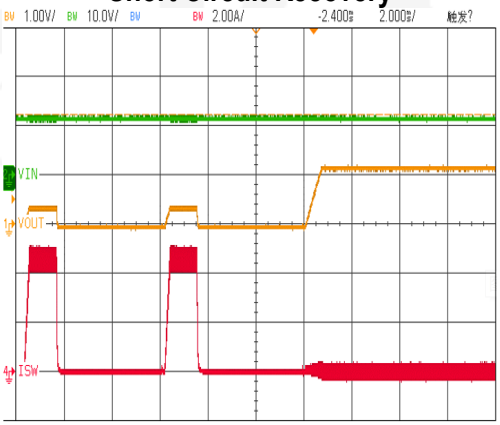
Load Transient
V_{IN}=12V,V_{OUT}=1.2V,I_{OUT}=0A to 1.5A



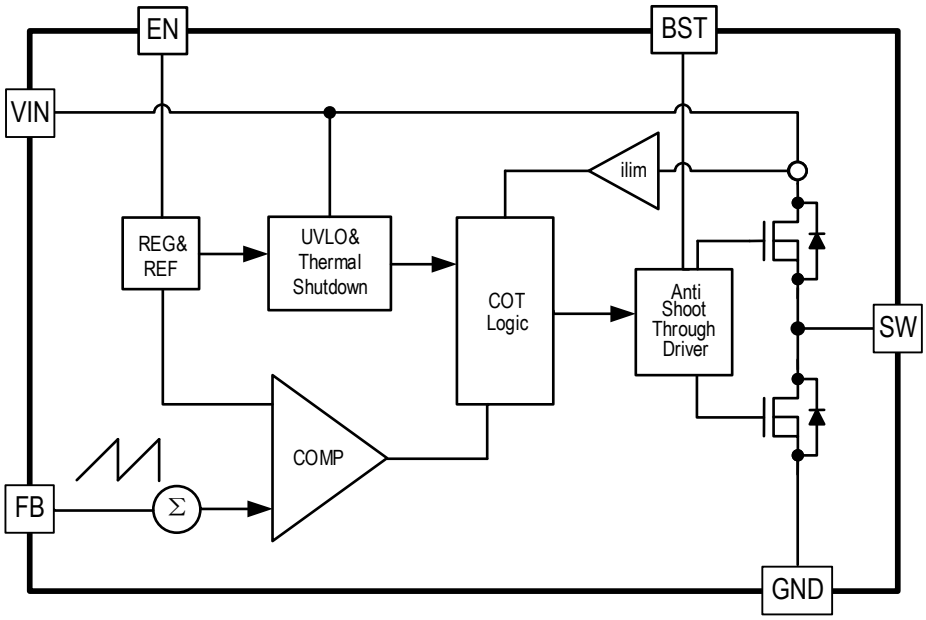
Short Circuit Protection



Short Circuit Recovery



FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The ETA8103 is a synchronous buck regulator ICs that integrates the adaptive COT control, top and bottom switches on the same die to minimize the switching transition loss and conduction loss.

ETA8103 is a wide input range, high-efficiency and high frequency DC-to-DC step-down switching regulator, capable of delivering up to 3A of output current. It adopts an Adaptive COT control scheme that enables very fast transient response and provides a very smooth transition when the output varies from light load to heavy load. It compares the sum of the FB voltage and a ripple voltage that mimics the voltage due to the output ESR and capacitance. The constant-on-time timer varies with line to achieve relative constant switching frequency across line.

Forced PWM Mode

A forced PWM DC-DC regulator always switches at a fixed frequency when the output heavy load or light load. This is to ensure a minimum output voltage ripple over the full load range.

Enable

EN is a digital control pin that turns the ETA8103 on and off. Drive EN High to turn on the regulator, drive it Low to turn it off. An internal 1MΩ resistor from EN pin to GND allows EN to float to shut down the chip. Connecting the EN pin through a pull up resistor or shorted EN to IN will automatically turn on the chip whenever plug in IN.

Over Current Protection and Hiccup

ETA8103 has a cycle-by-cycle over current limit for when the inductor current peak value is over the set current limit threshold. When the output voltage drop until FB falls below UV threshold (0.2V), the ETA8103 will enter hiccup mode. It will turn off the chip immediately for 4.5mS. After that, it will try to re-starts as normal for 1.5mS. After 1.5mS, if FB is still below UV threshold, then the chip enters hiccup mode again. If FB is higher than UV threshold, it will enter the normal mode.

Over-Temperature Protection

Thermal protection disables the output when the junction temperature rises to approximately 150°C, allowing the device to cool down. When the junction temperature cools to approximately 130°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits regulator dissipation, protecting the device from damage as a result of overheating.

APPLICATION INFORMATION

External Output Voltage Setting

In external Output Voltage Setting Version selected, the ETA8103 regulator is programmed by using an external resistor divider. The output voltage is calculated by using the below equation.

$$V_{OUT} = V_{REF} \times \ (1 + \frac{R_1}{R_2})$$

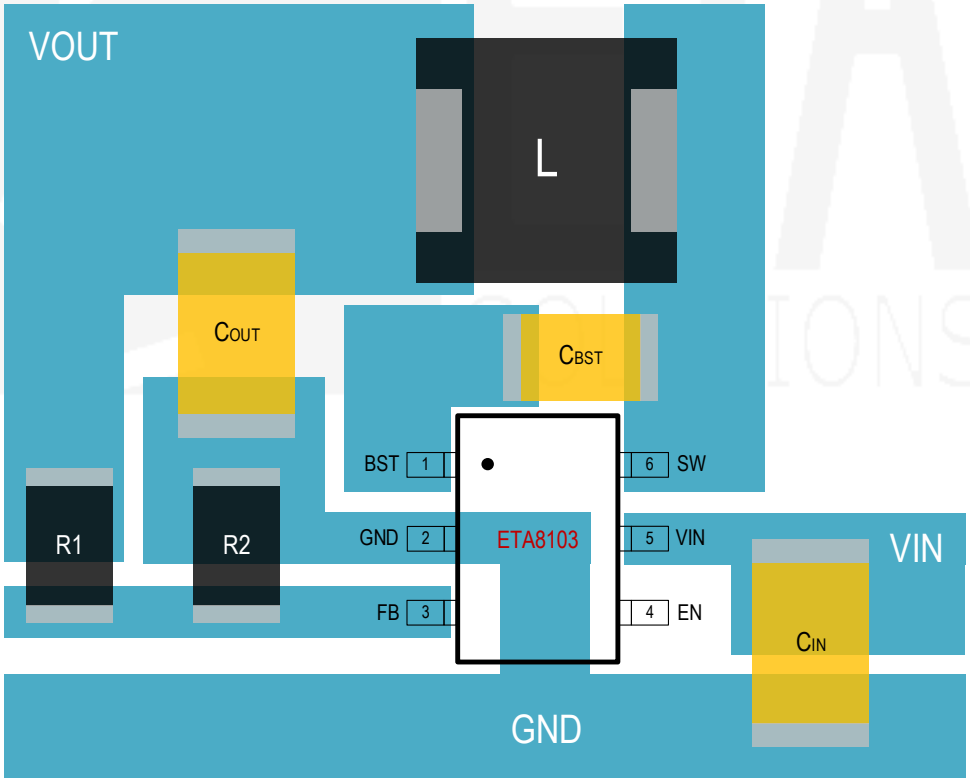
Where: VREF =0.6V typically (the internal reference voltage)

Resistors R2 has to be between 1KOhm to 20KOhm and thus R1 is calculated by the following equation.

$$R_1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R_2$$

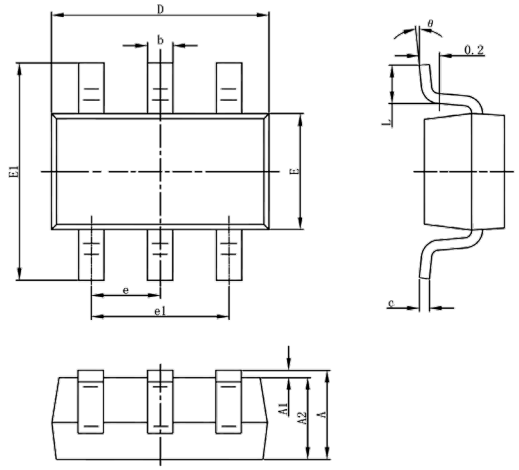
PCB LAYOUT GUIDE

Keep the power devices as close to the chip as possible to achieve the smallest power loop area, which leads to the best EMI performance; CIN is always placed nearest to VIN and GND.



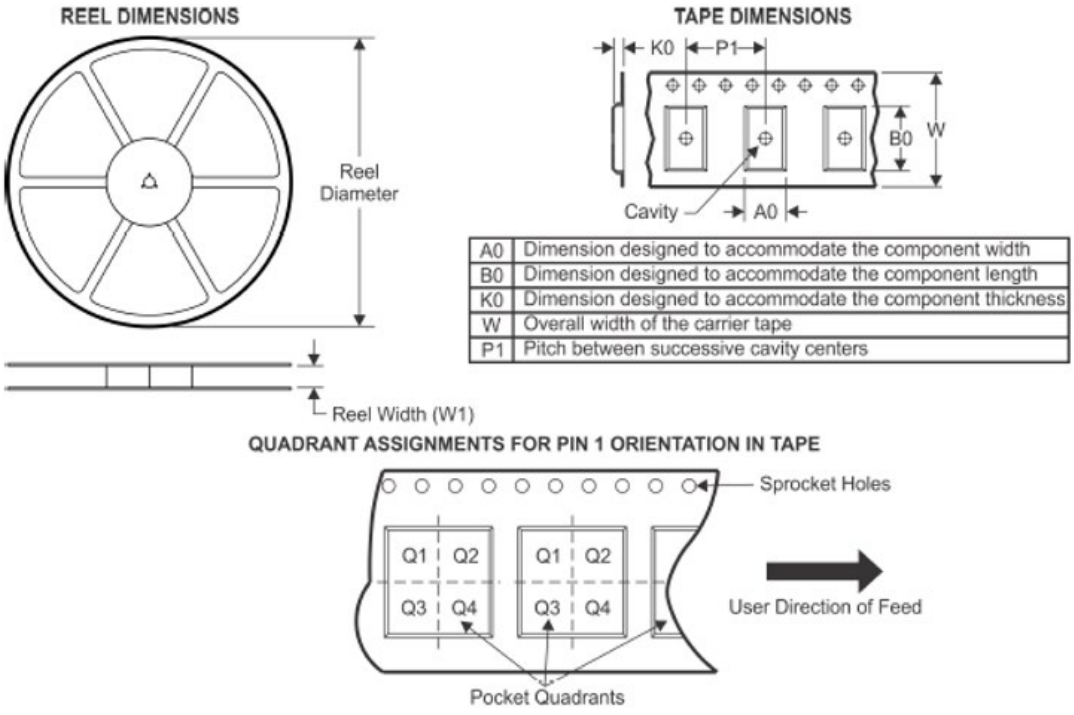
PACKAGE OUTLINE

Package: SOT23-6



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ETA8103S2G	SOT23-6	6	3000	180	9.5	3.17	3.23	1.37	4	8	Q3